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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Antonio Canova
Serial No.:	10/043,002
Filed:	January 9, 2002
For:	Process For Producing Printed Circuits And Printed Circuits Thus Otained
Group No.	3729
Attorney's Docket No.	N8125
Customer No.	23456

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Pursuant to 37 C.F.R. §1.56, applicant hereby calls to the attention of the Patent and Trademark Office the following patents and other documents which are listed on attached Form PTO-1449.

This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-reference application.

1. U.S. Patent No. 4,617,729 issued October 21, 1986, to Celnik.
2. U.S. Patent No. 4,873,764 issued October 17, 1989, to Grimm.
3. U.S. Patent No. 4,875,285 issued October 24, 1989, to Hann et al.
4. U.S. Patent No. 4,934,578 issued June 19, 1990, to Fritsch.
5. U.S. Patent No. 4,948,026 issued August 14, 1990, to Fritsch.
6. U.S. Patent No. 4,982,376 issued January 1, 1991, to Megens et al.
7. U.S. Patent No. 5,084,961 issued February 4, 1992, to Yoshikawa.

8. U.S. Patent No. 5,105,532 issued April 21, 1992, to Fritsch.

9. U.S. Patent No. 5,157,734 issued October 20, 1992, to Chen et al.

10. U.S. Patent No. 5,195,154 issued March 16, 1993, to Uchida.

11. U.S. Patent No. 5,220,724 issued June 22, 1993, to Gerstner.

12. U.S. Patent No. 5,250,469 issued October 5, 1993, to Tanaka et al.

13. U.S. Patent No. 5,258,738 issued November 2, 1993, to Schat.

14. U.S. Patent No. 5,321,885 issued June 21, 1994, to Hino et al.

15. U.S. Patent No. 5,323,528 issued June 28, 1994, to Baker.

16. U.S. Patent No. 5,349,504 issued September 20, 1994, to Simms et al.

17. U.S. Patent No. 5,377,405 issued January 3, 1995, to Sakurai et al.

18. U.S. Patent No. 5,410,801 issued May 2, 1995, to Shiloh et al.

19. U.S. Patent No. 5,413,275 issued May 9, 1995, to Verguld et al.

20. U.S. Patent No. 5,498,575 issued March 12, 1996, to Onishi et al.

21. U.S. Patent No. 5,563,572 issued October 8, 1996, to Hetzler.

22. U.S. Patent No. 5,659,947 issued August 26, 1997, to Eilers et al.

23. U.S. Patent No. 5,683,566 issued November 4, 1997, to Hetzler.

24. U.S. Patent No. 5,699,611 issued December 23, 1997, to Kurogi et al.

25. U.S. Patent No. 5,729,896 issued March 24, 1998, to Dalal et al.

26. U.S. Patent No. 5,896,081 issued April 20, 1999, to Tzeng et al.

27. U.S. Patent No. 5,974,661 issued November 2, 1999, to Neuhalfen.

28. U.S. Patent No. 6,151,771 issued November 28, 2000, to Tzeng et al.

29. Patent Abstract of Japan, vol. 14, no 99 (E-0893), 22 February 1990 regarding Publication No. 01303793 published July 12, 1989.

30. Patent Abstracts of Japan, volume and number unknown, regarding Japanese Abstract Publication No. 06196851 published July 15, 1994.

31. R. Keller; "Insights and observations on mixed-technology assembly" ELECTRONIC PACKAGING AND PRODUCTION., vol 28 no 4, April 1988, Massachussetts, pages 34-37, XP000140055.

32. Circuit Board Soldering Through Conformal Coating, Research Disclosure, Sept. 1988, no. 293, Kenneth Mason Publications

Copies of the listed documents are attached.

For foreign references:

1. PCT International Application (France), International Publication No. WO 95/13632 published May 18, 1995. Per the associated abstract, the relevance of this patent appears to be that it discloses a "[p]assive conductor component for surface mounting on a printed circuit board. The invention relates to a conductor component comprising a body with two substantially parallel conducting faces, the first face (24, 26) to be welded to a printed circuit board surface and the second face (22) designed to form an apparent conducting surface, a cavity being formed between the two faces. Application to surface-mounted printed circuit boards."

2. German Patent No. DE 44 25 803 A 1 issued July 21, 1994. Per the International Preliminary examination report, the relevance of this patent appears to be that the patent: "discloses a printed circuit board and a process for manufacturing such printed circuit board, the printed circuits comprising the following features: a laminar support, at least one electrically conductive trace on said laminar support, at least on auxiliary conductive element soldered to said conductive track (see column 2, lines 25 to 44), said auxiliary conductive

Applicant respectfully requests that these references be considered by the Examiner and made of record as part of the "available prior art" under 37 C.F.R. §1.104.

The Commissioner is authorized to charge any deficiency or credit any overpayment in connection with this Information Disclosure Statement to Deposit Account No. 23-0035.

Respectfully submitted,

David B. Pieper
Registration No. 42,998
WADDEY & PATTERSON
A Professional Corporation
Customer No. 23456
ATTORNEY FOR APPLICANT

David B. Pieper
Waddey & Patterson

414 Union Street, Suite 2020
Bank of America Plaza
Nashville, TN 37219
(615) 242-2400

CERTIFICATE OF FIRST CLASS MAILING

I hereby certify that this Information Disclosure Statement is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, April 10, 2002.

David B. Pieper

Registration No. 42,998

4/10/02

Date